

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

AKIYOSHI

Attorney Docket No: 108397-00025

Application No. 09/769,534

Art Unit: 2816

Filed: January 26, 2001

Examiner: T. Englund

For: POWER-ON RESET CIRCUIT METHOD FOR INITIALIZING AN INTEGRATED CIRCUIT (As Amended)

EXTRA CLAIMS FEE TRANSMITTAL

Commissioner for Patents
Washington, D.C. 20231

March 3, 2003

Sir:

Attached is an Amendment in the above-identified application.

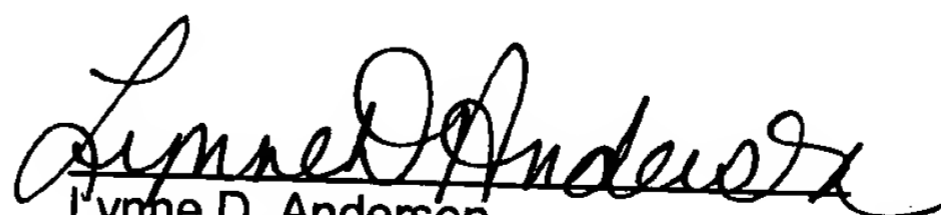
- ☐ Small entity status of this application under 37 C.F.R. §§1.9 and 1.27 has been established by a statement previously submitted.

The filing fee has been calculated as shown below.

	(Column 1)	(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN A SMALL ENTITY	
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADD'L FEE		RATE	ADD'L FEE
TOTAL CLAIMS	20 MINUS	20	=0	x 9	\$	OR	x 18	\$ 0
INDEP CLAIMS	15 MINUS	12	=3	x 42	\$		x 84	\$ 252
<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				+140	\$		+280	\$
					\$	OR		\$ 252

- ☒ Included in the attached check is the amount of \$252.00. The Commissioner is hereby authorized to charge any other fees that may be required to complete this filing, or to credit any overpayment, to Deposit Account No. 01-2300 referencing docket number 108397-00025.

Respectfully submitted,


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Art Unit: 2816

Filed: January 26, 2001

Examiner: T. Englund

For: POWER-ON RESET CIRCUIT METHOD FOR INITIALIZING AN INTEGRATED CIRCUIT (As Amended)

AMENDMENT AND RESPONSE UNDER 37 C.F.R. § 1.111

Commissioner for Patents
Washington, D.C. 20231

March 3, 2003

Sir:

In reply to the Office Action dated October 3, 2002, the period for response being extended to March 3, 2003 by the attached Petition for Extension of Time, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend claim 1, 3, 5, 7-11, 14 and 16 as follows:

1. (Twice Amended) A semiconductor integrated circuit comprising:
a sub reset signal generator for generating a plurality of sub power-on reset signals at timings different from each other; and
a main reset signal generator for generating a pulse signal including at least one rectangular pulse as a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-on reset signals.

3. (Twice Amended) A semiconductor integrated circuit comprising:
a sub reset signal generator for generating a sub power-on reset signal;

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